FCOG61BP Three-Phase Bipolar Firing Board

Features:

Industry Standard Digital LSI-Based Design

Fully Connectorized

Soft-Start and Soft-Stop Circuitry

Multiple Configurations Avaliable

Designed for Panel Mounting

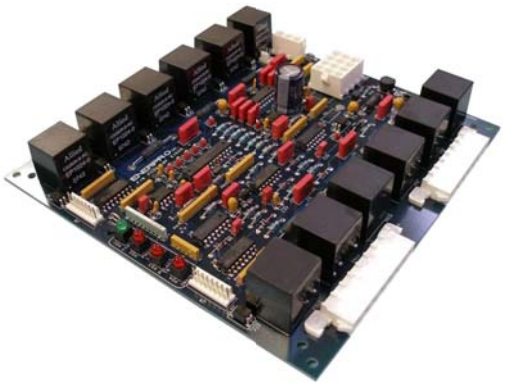
Complete SCR Assemblies Also Available

Applications:

Controlled Reversing Rectifier (Four-Quadrant)

Sequence Reversing AC Controller

Description
Based on our proven, time-tested FCOG6100 board, the FCOG61BP provides users the flexibility for reversing rectifiers and sequence-switching ac controllers. A polarity transition input allows users to invert the polarity of the rectifier with instant or timed polarity transition.



Operational Features
Analog Delay Angle Command Signal (SIG HI): Users may choose a variety of DC control signal ranges including 0-5 V, 4-20 mA, or custom ranges.

Soft-Start and Soft-Stop: Upon soft-start, SCR firing is enabled and the delay angle command ramps from the maximum value to the setpoint value determined by the SIG HI command signal. Upon soft-stop, the delay angle ramps from the setpoint value to the maximum value after which SCR firing is inhibited.

Instant Enable and Inhibit: A contact closure (relay, switch, transistor) instantly enables or inhibits SCR firing at the delay angle commensurate with the SIG HI command signal.

High Current Picket Fence Gate Drive: The transformer-isolated gate drive circuits provide a hard firing initial 15 V open circuit/1.5 A short circuit firing pulse followed by sustaining "back porch" pulses at 7 V open circuit/0.5 A short circuit. The gate pulse burst frequency is 384 times the mains voltage frequency.

Power-On Reset: A special circuit prevents unintentional SCR gating upon board power-up.

Phase loss inhibit: Thyristor gating is instantly inhibited when a phase loss is sensed on the ac mains; restoration of the mains voltage enables and soft-starts the unit.

Instant inhibit: Thyristor gating may be instantly inhibited with a contact closure (relay, switch, etc.)

Analog Delay Determinator Circuit: Enerpro's gate delay determinator circuit is based on an analog PLL circuit and implemented with a proprietary ASIC. This circuit adjusts the gate delay firing angle in negative proportion to the SIG HI delay angle command signal.

Polarity transition: Allows reversal of output voltage polarity via a simple contact closure. Upon ordering, customers may specify an instant polarity transition or a timed polarity transition depending upon specific applications.

Phase sequence insensitivity: SCR gating is unaffected by phase sequence.

Enhanced frequency insensitivity: A frequency compensation circuit reduces gate drive angle variance with respect to frequency. The gate drive angle decreases by approximately 5° for a frequency change from 60 Hz to 50 Hz, whereas older configurations exhibited a gate drive angle decrease of approximately 12.5°.

Board Construction: All circuit boards are assembled at the Enerpro plant in Goleta, California and are manufactured by a UL-approved fabricator from 2.4 mm thick FR4 fire resistant fiberglass epoxy laminate. All boards are conformal coated (MIL-1-46058, Type UR).

***Enerpro** applications engineers are available by e-mail or fax for applications assistance.*

FCOG61BP Product Datasheet	
Maximum Ratings	
AC mains voltage	600 Vac
Pulse transformer hipot	3500 Vac (60 seconds)
Operating temperature range	-5 C to 85 C
Board ac supply voltage	28 Vac (24 Vac nominal)
12 V regulator output current	20 mA (Note 1)
5 V reference output current	5 mA (Note 1)
Auxiliary control power available from 24 Vac/30 VDC outputs	10 W
Delay angle range	$10° \leq \alpha \leq 170°$
Electrical Characteristics	
Delay angle command signal (SIG HI)	Voltage: 0-5, 0.85-5.85, 0-10, 0-2V Current: 4-20 mA Or per customer specification
Delay angle reference phase shift	0° or -30° (application-specific)
Control signal isolation from ground	653 kΩ
Gate delay steady-state transfer function	Delay angle inversely proportional to delay angle command SIG HI
Gate delay dynamic transfer function bandwidth	-3 dB at 119 Hz, phase shift -45° at 68 Hz
Gate drive phase balance	±1° (max)
Delay angle variance	$\Delta(\alpha)/\Delta(f) = 0.5°/Hz$
Mains voltage distortion effect	Firing not affected by zero crossing; phase reference filter attenuation is 12.8 dB relative to fundamental at 5th harmonic
Lock acquisition time	30 ms (typ)
Soft-start/stop time (independently configurable)	0.05 - 20.0 s (typical)
Polarity transition inhibit time	0.06 - 20.0 s (typical)
Phase rotation effect	None
Phase loss inhibit	Automatic
Power-on inhibit	Automatic
Instant/soft inhibit/enable inputs	Dry contact
SCR gate pulse waveform (jumper selectable)	120° burst or 2-30° bursts, 30° spaced
Gate pulse burst frequency	384 times line frequency
Gate pulse width, 50 Hz	20-22 μs
Gate pulse width, 60 Hz	24-26 μs
Initial gate pulse open circuit voltage	15 V (30 VDC supply)
Sustaining gate pulse open circuit voltage	7.0 V (30 VDC supply)
Peak gate drive short circuit current	2.0 A (Notes 1 and 2)
Sustaining gate drive short circuit current	0.5 A (Notes 1 and 2)
Short-circuit gate drive current rise time	1.0 A/μs (Notes 1 and 2)

NOTES
1. With 30 Vdc nominal supply voltage
2. With 1.0 Ω non-inductive gate load

Ordering Guide		
Parameter	***Description***	***Code***
SCR Circuit Arrangement	*AC Controller* **1** Paralleled SCRs (Note 1) **2** 10 SCR Sequence Reversing (Note 1) *DC Converter* **3** 4-Quadrant 12 SCR **4** 4-Quadrant 12 SCR with Timed Transition Inhibit (Note 2)	
Parallel SCRs	**0** No **1** Yes	
Mains Frequency	**5/6** 50/60 Hz **XX** Specify (Note 3)	
SIG HI Delay Angle Command	**1** 0-5 V **2** 0.85-5.85 V **3** 0-10 V **4** 0-2 V **5** 4-20 mA **6** Other (specify)	
SCR Mains Voltage	**XX** Specify (Note 4)	
Phase References	**1** Onboard **2** External via header J7 (Note 5)	

NOTES
1 Specify circuit type on ordering documents
2 Specify required polarity transition timing
3 Specify as line frequency / 10, e.g., 120 Hz = 12
4 Specify as line voltage / 10, e.g., 480 V = 48
5 Connect attenuated ac mains @ J7 (properly attenuated by three external resistors) for phase reference

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